# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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**In re Application of :** Chaitanya Palusa

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| **Serial No. :** | 10/684,119 | **Group Art Un** | 2857 |
| **Filed :** | October 10, 2003 | **Examiner:** | Nguyen, V. |
| **For :** | IDDQ Test Methodology Based on the Sensivity of Fault Current to Power Supply Variations | **Atty Docket :** | B70885D / 00-513/1D |

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the date below:

Connie Del Castillo

5/27/04 Connie dellCastillo
Date Signature

## CERTIFICATION UNDER 37 C.F.R. 3.73(b)

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

LSI Logic Coporation, a Delaware corporation, certifies that it is the assignee of the entire right, title and interest in the patent application.

The undersigned has reviewed all the documents in the chain of title of the patent application identified above and, to the best of the undersigned's knowledge and belief, title is in the assignee identified above.

The undersigned (whose title is supplied below) is empowered to act on behalf of the assignee.

I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, inder Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Respectfully submitted,

Sandeep Jaggi
Chief IP Counsel
Corporate Assistant Secretary
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Date: 5/27/04